Architecture, Languages, Compilation and Hardware support for Emerging ManYcore systems
2nd Workshop, to be held as part of ICACS 2014

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Programmability at the verge of the manycore era

Massively parallel processors are made of hundreds to thousands cores, integrated memories and a dedicated network on a single chip. They provide high parallel performance while drastically reducing power consumption. Manycore architectures are therefore expected to enter both HPC (cloud servers, simulation, big data..) and embedded computing (autonomous vehicles, signal processing, cellular networks..). In the first session of this workshop, held together with ICCS 2013, we presented several academic and industrial works that contribute to the efficient programmability of manycores. This year, we also focus on preliminary user feedback to see if today available manycore processors meet their expectations.

In this session, we explore the newest academic and industrial works that contribute to the efficient programmability of manycores, and user feedbacks and insights on programming tools, their efficiency and soundness.

Topics of interest (not limited to)

• Programming languages and paradigms targeting massively parallel architectures
• Advanced compilers for programming languages targeting massively parallel architectures
• Advanced architecture support for massive parallelism management
• Advanced architecture support for enhanced communication for CMP/manycores
• Shared memory, data consistency models and protocols
• New OS, or dedicated OS for massively parallel application
• Runtime generation for parallel programing on manycores
• User feedback on existing manycore architectures

Homepage

https://sites.google.com/site/alchemyworkshop/

Important dates

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<tr>
<td>Full paper submission</td>
<td>December 15, 2013</td>
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<tr>
<td>Notification of acceptance</td>
<td>February 15, 2013</td>
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<tr>
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<td>March 5, 2013</td>
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<td>Workshop</td>
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Paper submission: up to 10 pages Elsevier format (single column)