Towards an automatic co-generator for manycores’ architecture and runtime: STHORM case-study

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Motivation

- Manycore architectures are difficult to explore
  - Large design space exploration
  - HW and SW modification for each new configuration
  - Lot of effort to reconfigure a new manycore architecture for simulation

- Need for an automatic co-generator for manycores’ architecture (HW) and runtime (SW)

- We will present a methodology for rapid generation of a manycore architecture (STHORM) model in SystemC, and its runtime, using IP-XACT description
Automatic flow
IP-XACT platform model

IP-XACT platform model input:
- System requirements and parameters
  - #PE, #memories, size mem, interconnections, etc...
- IP libraries in xml format
  - Processors, NoCs, standard bus interfaces, memories, etc..

Platform assembly using a software tool such as Magillem

IP-XACT platform model outputs 2 design configurations
- TLM level and RTL level interconnect abstractions
Platform generators

- Takes the manycore platform model in xml format

- Maps each component model to the correspond IP in the TLM/RTL libraries
  - take into account a set of parameters corresponding to the DSE iteration (such as the number of processors/clusters, degree of parallelism, custom IPs used, etc...).

- Configures the SW runtime of the manycore platform accordingly

- Using the IP-XACT standardized Tight Generator Interface (TGI) or JET workshop, automate the generation of:
  - TLM/RTL simulator + config parameters
  - SW Runtime + config parameters
  - Application + config parameters
  - Platform HAL and system memory map
Manycore architecture simulator

- SESAM for manycore architecture simulator
  - Acceleration of SystemC kernel (distributed engine)
  - Co-simulation with external tools such as Docea

- Generate statistics reports
  - Performance
  - Energy/power/Temperature
  - Reliability
Comparison of the resulting metrics with respect to the initial system requirements.

Based on the comparison results, the design optimization engine modifies the initial IP-XACT model parameters and even its specifications, based on heuristics (work in progress).
Massively parallel programmable (co-) processor

Multi-cluster architecture controlled by a Fabric Controller

Each cluster has:
- Up to 16 STxP70 PEs
- Hardware synchronizer
- Local memory
- CVPU
- CDMA
STHORM HAL + runtime + application

Hardware Abstraction Layer

**SYNCHRONIZATION APIs**
- `mutex.h`
- `barrier.h`
- `semaphore.h`

- `mutex_init()`, `mutex_lock()`, `mutex_unlock()`, etc.
- `sem_init()`, `sem_getvalue()`, `sem_wait()`, `sem_destroy()`, `Barrier_init()`, `barrier_sync()`, `barrier_destroy()`, etc.

- `ac_getval()`, `ac_setval()`
- `ac_postdec()`, `ac_postinc()`
- `ac_setsat()`, `acWritesreg()`, `ac_setval()`, etc.

**Generic runtime**

- Application
  - Execution engines
    - Multi-threading
    - Reactive Tasks Management
  - Resource management
    - HWS Resource management
    - DMA management
    - Memory management
    - Communication management
  - Hardware resources

**Application**

**CDFG**
Manycore simulator: STHORM in SESAM

STHORM Cluster 0
Conclusion and Future work

- We presented a methodology for automatic rapid generation of a manycore architecture model in SystemC, and its runtime, using IP-XACT description.
- STHORM architecture as case-study.

Next steps:
- Results analysis & design optimization
- Application configuration using pragmas
Thank you

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